Claims

[c1] 1.An integrated circuit structure utilizing fin-type field effect transistors (FinFETs) comprising:
a first FinFET having a first fin;
a second FinFET having a second fin running parallel to said first fin; and
an insulator fin positioned between source/drain regions of said first FinFET and said second FinFET, wherein said insulator fin has approximately the same width dimensions as said first fin and said second fin, such that the spacing between said first FinFET and said second FinFET is approximately equal to the width of one fin.

[c2] The integrated circuit structure in claim 1, further comprising a common gate formed over channel regions of said first FinFET and said second FinFET.

[c3] The integrated circuit structure in claim 2, wherein said common gate includes a first impurity doping region adjacent said first FinFET and a second impurity doping region adjacent said second FinFET.

[c4] The integrated circuit structure in claim 3, wherein differences between said first impurity doping region and

said second impurity doping region provide said common gate with different work functions related to differences between said first FinFET and said second FinFET.

[c5] The integrated circuit structure in claim 1, wherein said first fin and said second fin have approximately the same width.

[c6] An integrated circuit structure utilizing complementary fin-type field effect transistors (FinFETs) comprising:
a first-type of FinFET having a first fin;
a second-type of FinFET having a second fin running parallel to said first fin;
an insulator fin positioned between source and drain regions of said first first-type of FinFET and said second-type of FinFET, wherein said insulator fin has approximately the same width dimensions as said first fin and said second fin, such that the spacing between said first-type of FinFET and said second-type of FinFET is approximately equal to the width of one fin; and
a common gate formed over channel regions of said first-type of FinFET and said second-type of FinFET.

[c7] The integrated circuit structure in claim 6, wherein said common gate includes a first impurity doping region adjacent said first-type of FinFET and a second impurity doping region adjacent said second-type of FinFET.

[c8] The integrated circuit structure in claim 6, wherein differences between said first impurity doping region and said second impurity doping region provide said common gate with different work functions related to differences between said first-type of FinFET and said second-type of FinFET.

[c9] The integrated circuit structure in claim 6, wherein said first fin and said second fin have approximately the same width.

[c10] A method of forming pairs of parallel fin-type field effect transistors (FinFETs), said method comprising:
forming a semiconductor layer on a substrate;
forming a mandrel structure having substantially vertical sidewalls on said semiconductor layer;
forming a series of three layers of spacers on said sidewalls of said mandrel structure;
removing said mandrel structure and the middle spacer of said spacers, such that an inner spacer and an outer spacer remain extending from said semiconductor layer;
patterning said semiconductor layer, using said inner spacer and said outer spacer as masks such that regions protected by said inner spacer and said outer spacer remain as a first fin and a second fin extending from said substrate;

defining a channel region in said first fin and said second fin;
forming a gate conductor over a central region of said first fin and said second fin;
doping portions of said first fin and said second fin not protected by said gate conductor to form source and drain regions in said first fin and said second fin; and
insulating said source and drain regions of said first fin from source and drain regions of said second fin.

[c11] The method in claim 10, wherein said process of forming said series of three layers of spacers comprises:
forming said inner spacer along a sidewall of said mandrel structure;
forming said middle spacer on said inner spacer; and
forming said outer spacer on said middle spacer.

[c12] The method in claim 10, wherein said first fin comprises a first FinFET and said second fin comprises a second FinFET.

[c13] The method in claim 12, wherein said process of doping said source and drain regions implants different dopants at different angles into source and drain regions of said first FinFET and said second FinFET.

[c14] The method in claim 10, wherein said mandrel structure

includes two parallel sidewalls and wherein said method simultaneously forms pairs of FinFETs adjacent each of said sidewalls.

[c15] The method in claim 10, wherein said mandrel structure and said middle spacer comprise the same material, such that said removing process removes said mandrel and said middle spacer in a single process.

[c16] The method in claim 10, wherein said process of insulating said source and drain regions comprises depositing a dielectric material over said first fin and said second fin and removing said dielectric material from all areas except between said source and drain regions of said first fin and said second fin.

[c17] 17.A method of forming pairs of complementary parallel fin-type field effect transistors (FinFETs), said method comprising:
forming a semiconductor layer on a substrate;
forming a mandrel structure having substantially vertical sidewalls on said semiconductor layer;
forming a series of three layers of spacers on said sidewalls of said mandrel structure;
removing said mandrel structure and the middle spacer of said spacers, such that an inner spacer and an outer spacer remain extending from said semiconductor layer;

patterning said semiconductor layer, using said inner spacer and said outer spacer as masks such that regions protected by said inner spacer and said outer spacer remain as a first fin and a second fin extending from said substrate;
doping channel regions in said first fin and said second fin differently from one another using angled implantations;
forming a gate conductor over a central region of said first fin and said second fin;
doping portions of said first fin and said second fin not protected by said gate conductor to form source and drain regions in said first fin and said second fin; and
insulating said source and drain regions of said first fin from source and drain regions of said second fin.

[c18] The method in claim 17, wherein said doping of said channel regions comprises doping said first fin with a first channel doping species from an angle that is substantially perpendicular to said first fin such that said first fin protects said second fin from receiving said first channel doping species.

[c19] The method in claim 18, wherein said process of forming said semiconductor layer includes providing a second channel doping species within said semiconductor layer.

[c20] The method in claim 18, wherein said doping of said channel regions further comprises doping said second fin with a second channel doping species from an angle that is substantially perpendicular to said second fin such that said second fin protects said first fin from receiving said second channel doping species.

[c21] The method in claim 17, wherein said process of forming said series of three layers of spacers comprises:
forming said inner spacer along a sidewall of said mandrel structure;
forming said middle spacer on said inner spacer; and
forming said outer spacer on said middle spacer.

[c22] The method in claim 17, wherein said process of doping said source and drain regions implants different dopants at different angles into source and drain regions of said first fin and said second fin.

[c23] The method in claim 17, wherein said mandrel structure includes two parallel sidewalls and wherein said method simultaneously forms multiple parallel FinFETs adjacent each of said sidewalls.

[c24] The method and claim 17, wherein said mandrel structure and said middle spacer comprise the same material, such that said removing process removes said mandrel

and said middle spacer in a single process.

[c25] The method in claim 17, wherein said process of insulating said source and drain regions comprises depositing a dielectric material over said first fin and said second fin and removing said dielectric material from all areas except between said source and drain regions of said first fin and said second fin.

[c26] A method of forming parallel fin structures on a substrate comprising:
forming a mandrel structure having substantially vertical sidewalls on said semiconductor layer;
forming a series of three or more layers of spacers on said sidewalls of said mandrel structure; and
removing said mandrel structure and the alternate layers of said spacers, such that an inner spacer and an outer spacer remain extending from said substrate.

[c27] The method in claim 26, wherein said inner spacer and said outer spacer comprise one of: conductors; semiconductors; insulators; and mask elements used to pattern features into said substrate.

[c28] The method in claim 26, wherein said process of forming said series of three layers of spacers comprises:
forming said inner spacer along a sidewall of said man-

drel structure;
forming said middle spacer on said inner spacer; and
forming said outer spacer on said middle spacer.

[c29] The method in claim 26, wherein said spacers all have approximately the same width, such that said inner spacer is separated from said outer spacer by the width of one spacer.

[c30] A method of forming parallel structures on a substrate comprising:
forming a layer of material on said substrate;
forming a mandrel structure having substantially vertical sidewalls on said layer of material;
forming a series of three layers of spacers on said sidewalls of said mandrel structure;
removing said mandrel structure and the middle spacer of said spacers, such that an inner spacer and an outer spacer remain extending from said layer of material; and
patterning said layer of material using said inner spacer and said outer spacer as masks, such that regions protected by said inner spacer and said outer spacer remain as a first fin and a second fin extending from said substrate.

[c31] The method in claim 30, wherein said layer of material comprises one of: conductors; semiconductors; and in-

sulators.

[c32] The method in claim 30, wherein said process of forming said series of three layers of spacers comprises:
forming said inner spacer along a sidewall of said mandrel structure;
forming said middle spacer on said inner spacer; and
forming said outer spacer on said middle spacer.

[c33] The method in claim 30, wherein said spacers all have approximately the same width, such that said inner spacer is separated from said outer spacer by the width of one spacer.